(54) Title: APPARATUS FOR PROVIDING A VIDEO LIP SYNC DELAY AND METHOD THEREFORE
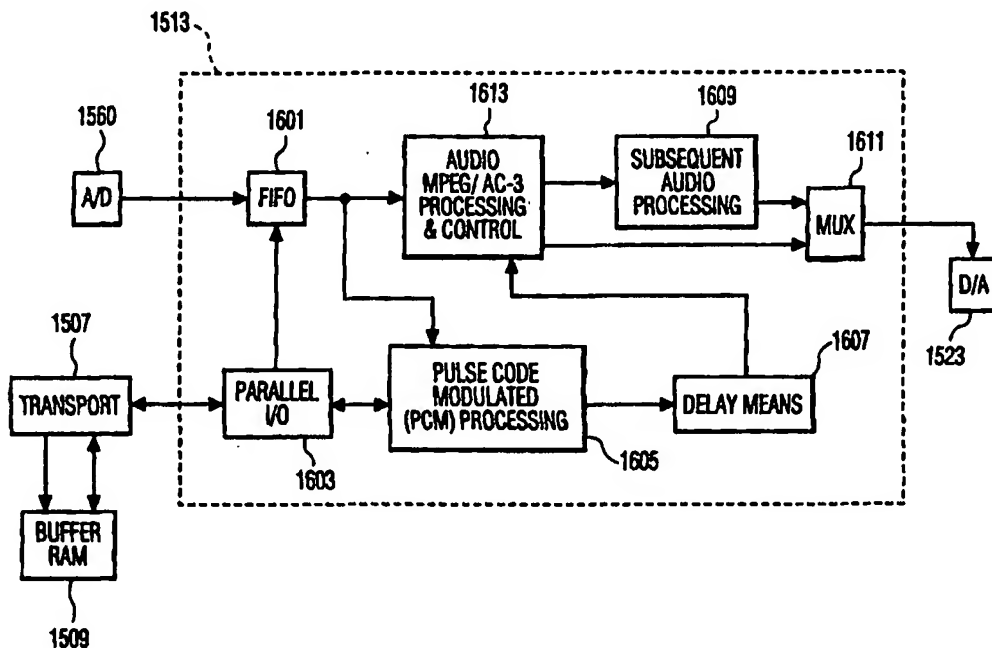
(57) Abstract

    A digital receiver for processing one of a packetized input data stream and a digitized standard definition input signal provides a delay in the processing of the standard definition audio input signal to maintain synchronism with the processing of a corresponding standard definition video signal.

APPARATUS FOR PROVIDING A VIDEO LIP SYNC DELAY AND METHOD THEREFORE

Field of the Invention

The invention concerns an apparatus for providing a delay of a standard definition television ("SDTV") (e.g., NTSC, PAL or SECAM) audio signal to maintain proper synchronization of the video image and the audio output. The invention is especially well suited for use in a high definition television ("HDTV") system.

Background of the Invention

Typical consumer electronic products, such as televisions and VCRs are known to be configured to receive standard definition signals (such as NTSC, PAL or SECAM). However, it is recognized that the emerging digital consumer electronic products must be configured to receive both digital streams and standard definition signals. Digital receivers are designed to receive television information in the form of a stream of digital packets representing video and audio information in compressed form in accordance with a predetermined digital compression standard. For example, the MPEG video and audio compression standards may be employed. The MPEG video and audio compression standards are international standards for the coded representation of and audio information developed by the Motion Pictures Expert Group.

Summary of the Invention

The present invention resides in part in the recognition that a high definition digital receiver (e.g., HDTV) configured to receive SDTV signals is subject to displaying a video image that is not in synchronization with the audible output and in part with the apparatus to maintain synchronization.

In accordance with one aspect of the present invention, a receiver apparatus comprises means for receiving a packetized input data

stream; means for receiving a digitized audio signal and a digitized video signal; and means for partitioning said packetized data stream to generate a video component and an audio component. Further, the apparatus comprises a first and second means for digital signal

5   processing to generate, respectively, a decompressed video output signal in response to one of said video component of said packetized data stream and said digitized video signal and a decompressed audio output signal in response to one of said audio component of said packetized data stream and said digitized audio signal. Still further,

10   the apparatus comprises a means for transposing said video output signal to a displayable video signal and said audio output signal to an audible output signal.

In accordance with another aspect of the present invention, the

15   receiver apparatus further comprises an adjustable means for delaying said output audio signal to be in synchronism with said displayable video signal.

In accordance with yet another aspect of the present invention, the

20   adjustable delaying means comprises an adjustable memory device and may be connected to one of the second processing means or the partitioning means. The second processing means further comprises means for secondary audio processing., such as surround sound processing.

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In accordance with a method aspect of the present invention, there is provided a method for processing an input signal comprising; receiving one of a packetized input data stream and a digitized signal comprised of a digitized video signal and a digitized audio signal;

30   partitioning one of said packetized data stream to generate a video component and an audio component; converting said digitized video signal into a progressive scan format; processing one of said packetized data stream and said digitized input signal to generate a decompressed video and audio output signal; and transposing said

35   video output signal to a displayable video signal and said audio output signal to an audible output signal.

In accordance with another method aspect of the present invention, the method for processing an input signal further comprises delaying said audio output signal to be in synchronism with said displayable video signal. The step of delaying comprises providing said audio

5   output signal to an adjustable memory device or to a secondary processor.

These and other aspects of the invention will be described with respect to the accompanying Drawings.

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Brief Description of the Drawing

Figure 1 is a simplified schematic block diagram of a digital receiver including apparatus constructed in accordance with

15   an exemplary embodiment of the present invention; and

Figure 2 is a simplified schematic block diagram of the audio MPEG/AC-3 decoder of Figure 1.

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Detailed Description of the Drawing

Digital receiver 15 tunes, demodulates and otherwise processes the received television signal as will be described in detail below to produce displayable video images on a conventional display device

25   and audible signals on conventional speakers in response to received television information.

The apparatus shown in Figure 1 is a digital receiver 15, such as, for example, one that may be employed in a high definition television

30   ("HDTV"). Particularly, the television information is received in either (1) compressed form in accordance with a predetermined digital compression standard (for example, the MPEG video and audio compression standards) or (2) SDTV analog signal (for example, NTSC, PAL or SECAM). The MPEG video and audio compression standards

35   are international standards for the coded representation of and audio information developed by the Motion Pictures Expert Group.

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The digital video and audio signals are compressed and encoded according to the MPEG video and audio compression and encoding standards to form respective series or streams of data packets. The video and audio packets are multiplexed to form a stream of packets

5   for transmission. Each packet of the transmission stream includes a data or "payload" portion and a header portion which identifies the type of information represented by the payload portion of the packet. Packets corresponding to control and other data may also be added the transmission stream.

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Forward error correction (FEC) data is added to the packets in order make the correction of errors due to noise within the transmission path possible. The well known Viterbi and Reed-Solomon types of forward error correction coding may both be advantageously

15   employed. The digital information resulting from the compression, encoding and error correction operations is modulated on a carrier in what is known in the digital transmission field as QPSK (Quadrature Phase Shift Keying) modulation.

20   Digital receiver 15 includes both a HD/NTSC tuner 1500 and a DSS tuner 1501, both having a local oscillator and mixer (not shown) for selecting the appropriate carrier signal form the plurality of received signals and for converting the frequency of the selected carrier to a lower frequency to produce an intermediate frequency (IF) signal.

25   Further HD/NTSC tuner 1500 and DSS tuner 1501 demodulate the IF signal.

DSS tuner 1501 may include a QPSK demodulator, not shown, to produce a demodulated digital signal and a FEC decoder, not shown, to

30   decode the error correction data contained in the demodulated digital signal, and based on the error correction data corrects the demodulated packets representing video, audio and other information to produce a stream of error corrected data packets which are provided to link circuitry 1505. The SDTV demodulated signal from

35   HD/NTSC tuner 1500 is further processed in a conventional manner by NTSC processing circuitry 1540. (The details of NTSC processing circuitry 1540 are not required to fully understand the present

invention.)　Whereas, the HD demodulated stream is provided the link circuitry 1505.

A MPEG transport decoder unit 1507 cooperates with a buffer memory in the form of a random access memory (RAM) 1509 to route the payload portion of the video packets of the error corrected stream to a video MPEG decoder 1511 and the payload portion of the audio packets to an audio MPEG/AC-3 decoder 1513 via a data bus or separate lines according to the header information contained in the packets. RAM 1509 is used to temporarily store packets of the data stream of the transmitted signal in respective memory locations in accordance with the type of information which they represent. Transport unit 1507 is a memory manager for buffer RAM 1509 which demultiplexes the data packets of the error corrected stream and routes the payload portions of the packets to respective memory locations according to the header portions of the respective packets. The contents of the video and audio sections of RAM 1509 are read out and transferred to video MPEG decoder 1511 and audio MPEG/AC-3 decoder 1513, respectively, on demand in response to requests from these units. Details of the construction of transport 1507 and buffer RAM 1509 are not required to understand the present invention, but may be found in US patent application serial number 232,789, entitled "A Packet Video Signal Inverse Transport System" filed for M. S. Deiss on April 22, 1994.

Video MPEG decoder 1511 interfaces with a dynamic random access memory (DRAM) 1515 to decode and decompress the payload portion of the video packets to form a stream or sequence of digital words representing video information in component form. For example, the components may correspond to a luminance (Y) component and two color difference (Cr and Cb) components. Further, video MPEG decoder 1511 has a separate input to receive a digitized SDTV video signal from analog-to-digital converter ("A/D") 1550. (Details of the construction of video MPEG decoder is not required to understand the present invention.) Video decoding and decompression integrated circuits (ICs) are commercially available. For example, a MPEG decoding and decompression IC, identified by part number ST3240, is available from SGS Thomson, of France.

The luminance and chrominance representative digital words are converted to analog luminance and chrominance signals by respective sections of a digital-to-analog converter (DAC) 1519.

5   These analog luminance and chrominance signals are coupled to "2H" video processing circuitry 1529 which converts the component representative digital words to three separate video signals; R, G and B. These video signals are provided to a display device 1531. (Details of the construction of the well known "2H" video processing circuitry

10 and display device are not required to understand the present invention.)

Audio MPEG/AC-3 decoder 1513 interfaces with dynamic random access memory (DRAM) 1521 to decode and decompress the payload

15 portion of the audio packets to produce a sequences of digital words representing "left" (L) and "right" (R) audio information. As is well known in the art, memory 1521 may optionally be integral with audio MPEG/AC-3 decoder 1513. Further, decoder 1513 has a separate input to receive a digitized standard definition audio signal

20 (explained in detail below in connection with Figure 2a). Audio decoding and decompression ICs are commercially available. For example, a MPEG audio decoding and decompression IC, identified by part number DSP56011, is available from Motorola. The sequences of audio representative digital words are converted to baseband analog

25 left and right audio signals by respective sections of DAC 1523 and audio processing circuitry 1525. Although only two audio channels are shown in the Figure, it will be appreciated that in practice, one or more additional audio channels, for example, for "surround sound" reproduction, may be provided.

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The baseband analog video and audio signals are coupled to speakers 1527, which may be integral with display device 1531 via respective baseband connections. The baseband analog video and audio signals may also be coupled to a modulator (not shown) which modulates the

35 analog signals on to a radio frequency (RF) carrier in accordance with a conventional television standard such as NTSC, PAL or SECAM for coupling to the antenna input of a display device without baseband inputs.

A microprocessor 1527 provides frequency selection control data to HD/NTSC tuner 1500 and DSS tuner 1501 for controlling the operation of the tuner to tune channels selected by the user. Microprocessor 1527 also operates interactively with transport 1507 to affect the routing of payload portions of packets. Microprocessor 1527 additionally provides control data to video MPEG decoder 1511 and audio decoder 1513 via a control bus. Microprocessor 1527 operates in response to a control program stored in a "read only" memory (ROM) 1529.

Both video MPEG decoder 1515 and audio MPEG/AC-3 decoder 1513 are configured to receive the digitized video and audio components, respectively, of a SDTV analog input signal. Digitized video and audio components are provided by passing the demodulated and processed analog video and audio components generated by NTSC processing circuitry through analog-to-digital converters 1550 and 1560, respectively. In operation, the digitized video component is processed by the video MPEG decoder and up-converter 1511 and the digitized audio component is processed by audio MPEG/AC-3 decoder 1513. The time to process the digitized video component is greater than the time necessary to process the digitized audio component thereby creating a delay between audio output and the display image.

The apparatus shown in Figure 2 is a simplified schematic block diagram of the audio MPEG/AC-3 decoder 1513 discussed above. As described above, decoder 1513 generates digital words which represent the audio information in response to either a digitized SDTV audio signal produced by A/D 1560 or the audio portion of the input stream produced by MPEG transport decoder unit 1507 and RAM 1509. The details of audio MPEG/AC-3 decoder 1513 will be discussed in terms of it functional operation and signal flow path. The audio portion of the input MPEG stream is supplied to decoder 1513 through parallel input/output 1603. The input stream is provided to FIFO memory means 1601 for initial processing and formatting. Audio MPEG/AC-3 Processing circuitry 1613 processes the input stream to produce sequences of digital words representing the audio information. Additional audio processing, such as surround

sound processing, may be performed by subsequent audio processing means 1609 to produce further processed audio information. A control signal (not shown) is provided multiplexer ("MUX") 1611 to select between the audio information generated by processing and

5   control circuitry 1613 and the further processed audio information generated by subsequent audio processing means 1609.

Audio MPEG/AC-3 decoder 1513 is configured to generate audio information in response to a digitized SDTV audio input signal

10   received from A/D 1560 as described above. FIFO memory means 1601 formats the digitized audio input signal prior to it being provided to pulse code modulated circuitry 1605. As discussed above, the time to process the digitized SDTV audio input signal is less than the time necessary to process the corresponding digitized video

15   signal thereby necessitating the insertion of a delay in the audio processing to maintain synchronization between these two signals. The PCM processed audio input signal is provided to delay means 1607. Delay means 1607 may be a portion of the general memory 1521 associated with the audio MPEG/AC-3 decoder 1513. The

20   delayed audio input signal is provided to the control portion of audio MPEG/AC-3 processing circuitry 1613 and may either be supplied directly to MUX 1611 or to subsequent audio processing means 1609 as described above prior to being supplied to D/A 1523.

25   Alternately, the PCM processed audio signal may be provided to transport unit 1507 and RAM 1509 through parallel I/O 1603 for delay processing. Specifically, RAM 1509 will be used to achieve the delay accomplished by delay means 1607 as described above.

30   While the present invention has been described in terms of a specific embodiment, it will be appreciated that modifications may be made. These and other modifications are contemplated to be within the scope of the invention defined by the following claims.

CLAIMS

1. A receiver comprising:

(a) means for receiving a packetized input data stream comprised of multiplexed and compressed packets, each of said packets having at least header and payload data;

(b) means for receiving a digitized audio signal and a digitized video signal;

(c) means for partitioning said packetized data stream to generate a video component and an audio component;

(d) first means for digital signal processing to generate a decompressed video output signal in response to one of said video component of said packetized data stream and said digitized video signal;

(e) second means for digital signal processing to generate a decompressed audio output signal in response to one of said audio component of said packetized data stream and said digitized audio signal; and

(f) means for transposing said video output signal to a displayable video signal and said audio output signal to an audible output signal.

2. The receiver of claim 1 further comprising an adjustable means for delaying said output audio signal to be in synchronism with said displayable video signal.

3. The receiver of claim 2 wherein said adjustable delaying means comprises an adjustable memory device.

4. The receiver of claim 3 wherein said delaying means is connected to said second processing means.

5. The receiver of claim 3 wherein said delaying means is connected to said partitioning means.

6.   The receiver of claim 4 or claim 5 wherein said second
processing means further comprises means for secondary audio
processing.

5   7.   The receiver of claim 6 wherein said secondary audio
processing means comprises means for surround sound processing.

8.   The receiver of claim 1 or claim 7 wherein said first processing
means comprises a means for converting said digitized video signal
10   having an interlace video format into a digitized video signal having a
progressive scan format.

9.   A method for processing an input signal having a video
component and an audio component, said method comprising:
15   (a)   receiving one of a packetized input data stream and a
digitized signal comprised of a digitized video signal and a digitized
audio signal;
             (b)   partitioning one of said packetized data stream to
generate a video component and an audio component;
20   (c)   converting said digitized video signal into a progressive
scan format;
             (d)   processing one of said video component of said packetized
data stream and said digitized video signal to generate a
decompressed video output signal;
25   (e)   processing one of said audio component of said packetized
data stream and said digitized audio signal
to generate a decompressed audio output signal,
             (f)   transposing said video output signal to a displayable video
signal and said audio output signal to an audible output signal.
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10.   The method of claim 9 further comprising delaying said audio
output signal to be in synchronism with said displayable video signal.

11.   The method of claim 10 wherein the step of delaying comprises
35   providing said audio output signal to an adjustable memory device.

12.   The method of claim 11 further comprising the step of
providing said audio output signal to a secondary processor.
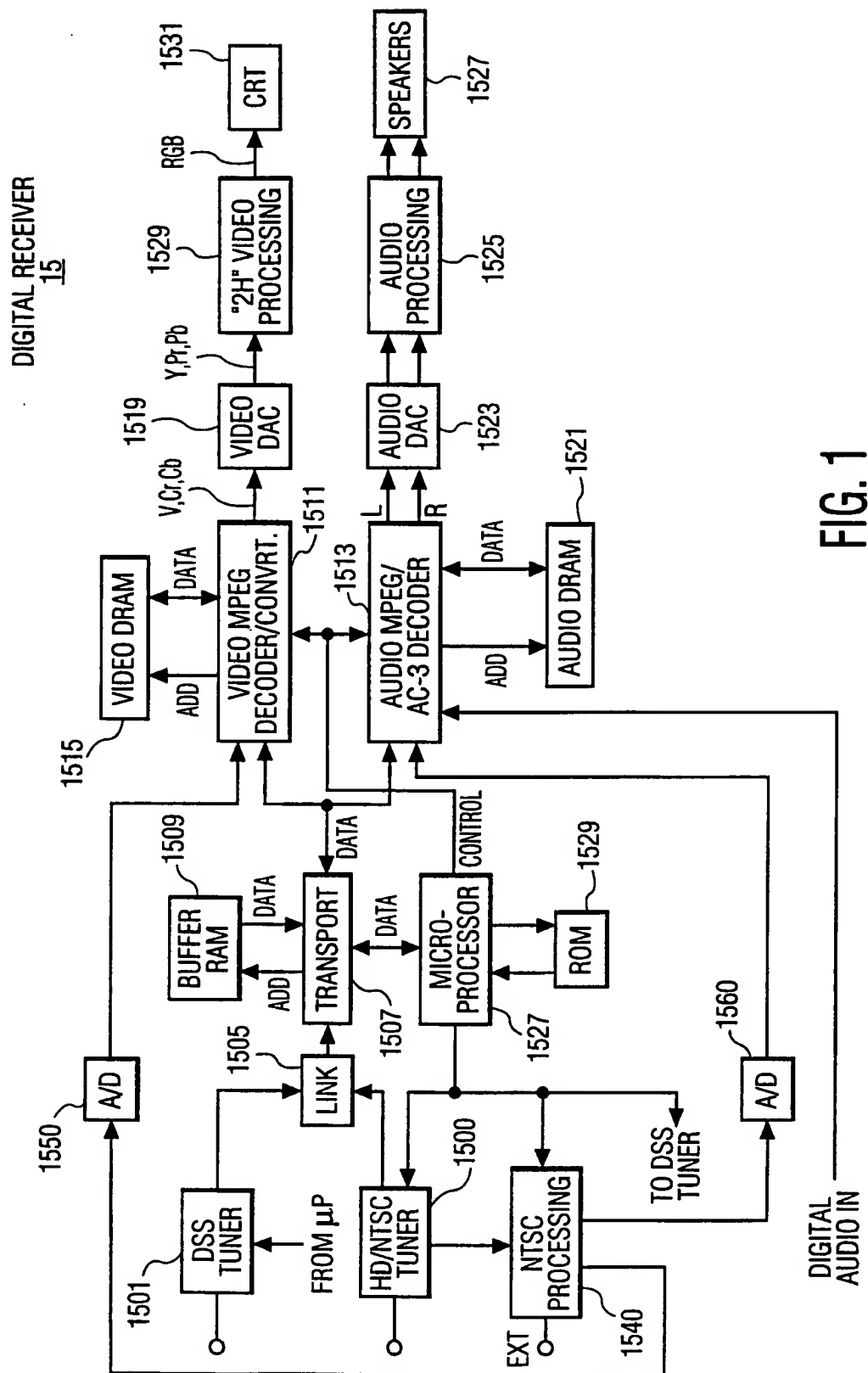
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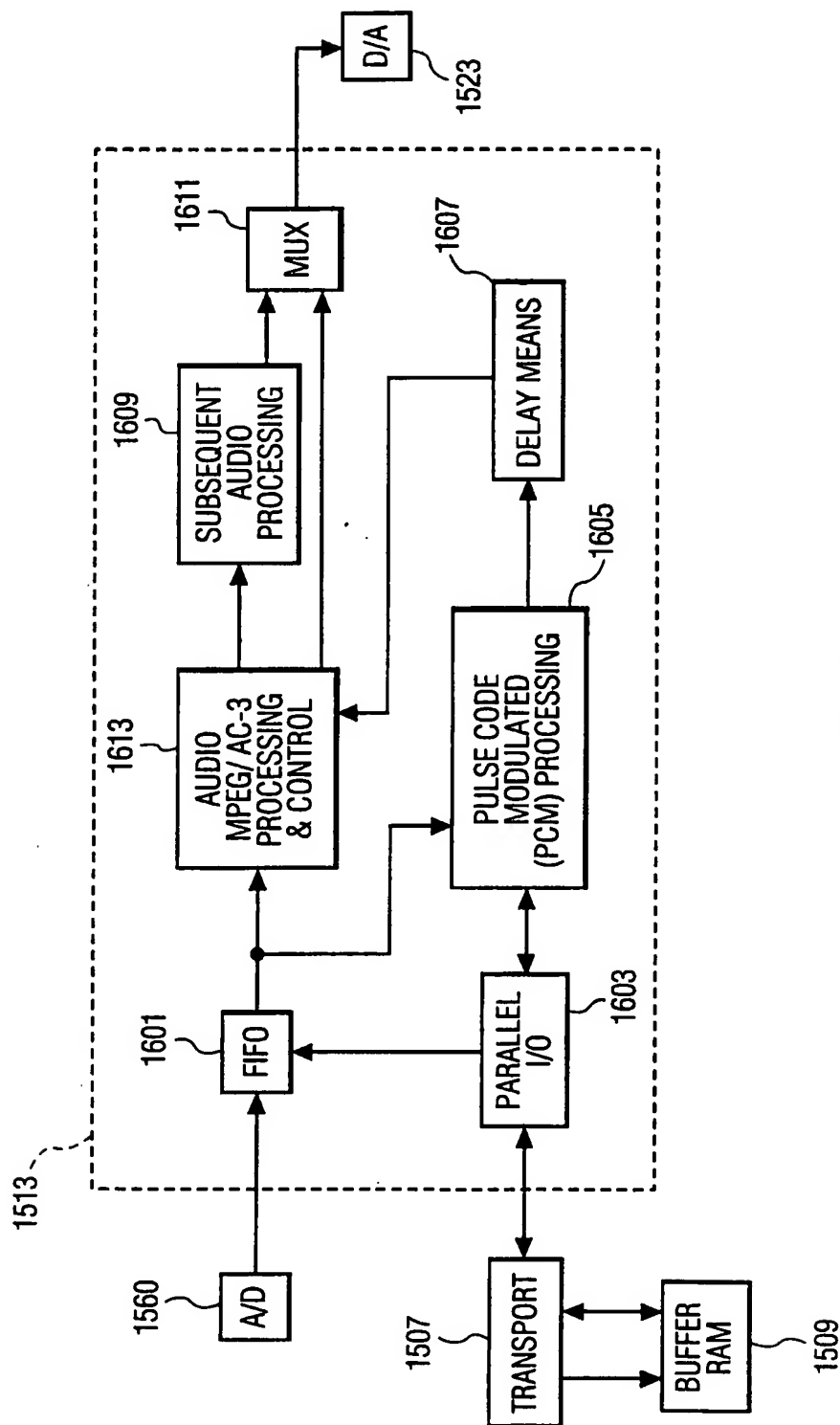DIGITAL RECEIVER
15

FIG. 1

FIG. 2

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6   H04N5/04   H04N5/44   H04N5/60   H04N7/52

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6   H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 766 462 A (SAMSUNG ELECTRONICS CO LTD) 2 April 1997	1,9
Y	see page 2, line 13 - page 3, line 23	2,3,6-8, 10-12
	see column 16, line 5 - column 17, line 11; figure 8	

Y	EP 0 776 134 A (GEN INSTRUMENT CORP) 28 May 1997 see abstract	2,3,10, 11

Y	EP 0 598 295 A (MATSUSHITA ELECTRIC IND CO LTD) 25 May 1994 see abstract	2,3,10, 11

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[X] Further documents are listed in the continuation of box C.   [X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 April 1999	06/05/1999

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INTERNATIONAL SEARCH REPORT

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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